TelCom Semiconductor, Inc.

TC9400
TC9401
TC9402

VOLTAGE-TO-FREQUENCY/FREQUENCY-TO-VOLTAGE CONVERTERS

FEATURES

Voltage-to-Frequency

- **Choice of Guaranteed Linearity:**
  - **TC9401 .... 0.01%**
  - **TC9400 .... 0.05%**
  - **TC9402 .... 0.25%**
- **DC to 100 kHz (F/V) or 1Hz to 100kHz (V/F)**
- **Low Power Dissipation .... 27mW Typ**
- **Single/Dual Supply Operation .... + 8V to + 15V or ± 4V to ± 7.5V**
- **Gain Temperature Stability .... ± 25 ppm/°C Typ.**
- **Programmable Scale Factor**

Frequency-to-Voltage

- **Operation .... DC to 100kHz**
- **Choice of Guaranteed Linearity:**
  - **TC9401 .... 0.02%**
  - **TC9400 .... 0.05%**
  - **TC9402 .... 0.25%**
- **Programmable Scale Factor**

APPLICATIONS

- **µP Data Acquisition**
- **13-Bit Analog-to-Digital Converters**
- **Analog Data Transmission and Recording**
- **Phase-Locked Loops**
- **Frequency Meters/Tachometer**
- **Motor Control**
- **FM Demodulation**

GENERAL DESCRIPTION

The TC9400/TC9401/TC9402 are low-cost voltage-to-frequency (V/F) converters utilizing low power CMOS technology. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

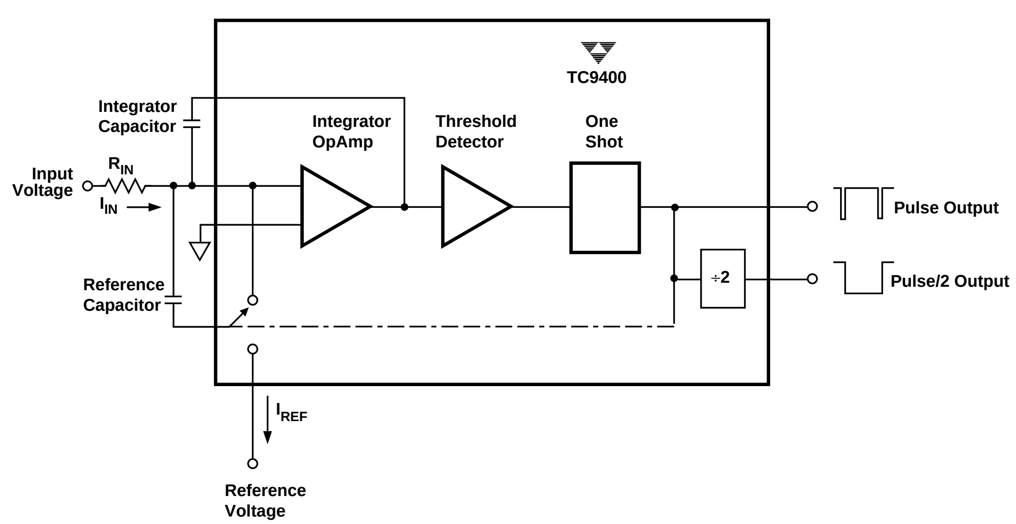
The devices can also be used as highly-accurate frequency-to-voltage (F/V) converters, accepting virtually any input frequency waveform and providing a linearly-proportional voltage output.

A complete V/F or F/V system only requires the addition of two capacitors, three resistors, and reference voltage.

ORDERING INFORMATION

Part No.	Linearity (V/F)	Package	Temperature Range
TC9400COD	0.05%	14-Pin SOIC (Narrow)	0°C to +70°C
TC9400CPD	0.05%	14-Pin Plastic DIP	0°C to +70°C
TC9400EJD	0.05%	14-Pin CerDIP	– 40°C to +85°C
TC9401CPD	0.01%	14-Pin Plastic DIP	0°C to +70°C
TC9401EJD	0.01%	14-Pin CerDIP	– 40°C to +85°C
TC9402CPD	0.25%	14-Pin Plastic DIP	0°C to +70°C
TC9402EJD	0.25%	14-Pin CerDIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

$V_{DD} - V_{SS}$ .... +18V
I_{IN} 10mA
V_{OUT} Max $-V_{OUT}$ Common 23V
$V_{REF} - V_{SS}$ .... – 1.5V
Storage Temperature Range .... – 65°C to +150°C
Operating Temperature Range
 C Device .... 0°C to +70°C
 E Device .... – 40°C to +85°C
Package Dissipation ($T_A \leq 70°C$)
 8-Pin CerDIP 800mW
 8-Pin Plastic DIP 730mW
 8-Pin SOIC 470mW
Lead Temperature (Soldering, 10 sec) .... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = – 5V, V_{GND} = 0V, V_{REF} = – 5V, R_{BIAS} = 100kΩ, Full Scale = 10kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified (– 40°C to +85°C for E device, 0°C to +70°C for C device).

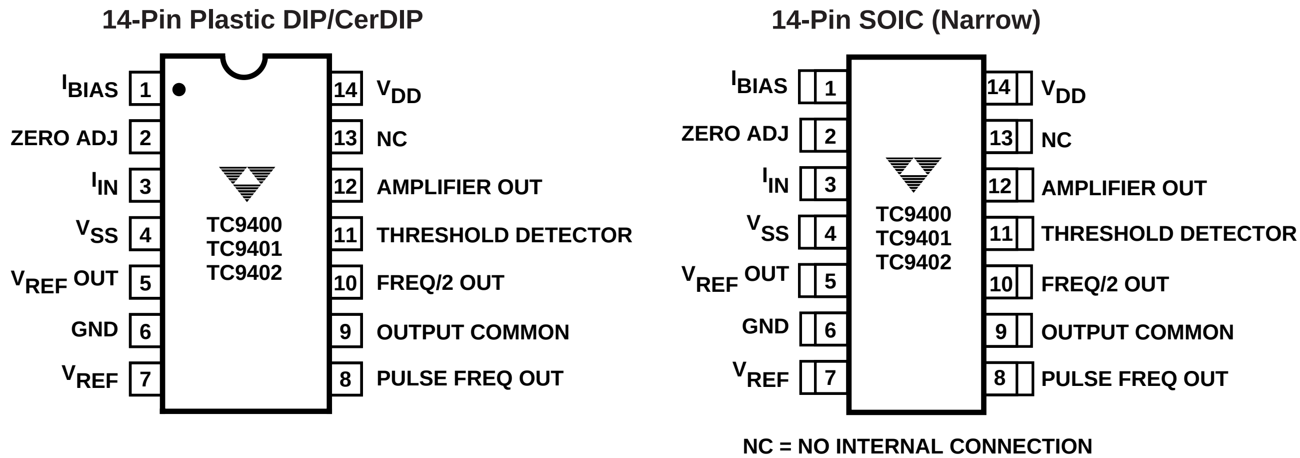
VOLTAGE-TO-FREQUENCY		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Accuracy											
Linearity 10 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	0.004	0.01	—	0.01	0.05	—	0.05	0.25	% Full Scale
Linearity 100 kHz	Output Deviation From Straight Line Between Normalized Zero Reading and Full-Scale Input	—	0.04	0.08	—	0.1	0.25	—	0.25	0.5	% Full Scale
Gain Temperature Drift (Note 1)	Variation in Gain A Due to Temperature Change	—	± 25	± 40	—	± 25	± 40	—	± 50	± 100	ppm/°C Full Scale
Gain Variance	Variation From Ideal Accuracy	—	± 10	–	—	± 10	—	—	± 10	–	% of Nominal
Zero Offset (Note 2)	Correction at Zero Adjust for Zero Output When Input is Zero	—	± 10	± 50	—	± 10	± 50	—	± 20	± 100	mV
Zero Temperature Drift (Note 1)	Variation in Zero Offset Due to Temperature Change	—	± 25	± 50	—	± 25	± 50	—	± 50	± 100	µV/°C
Analog Input											
I_{IN} Full Scale	Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	10	—		10	—	µA
I_{IN} Overrange	Overrange Current	—	—	50	—	—	50	—	—	50	µA
Response Time	Settling Time to 0.1% Full Scale	—	2	—	—	2	—	—	2	—	Cycle
Digital Section											
V_{SAT} @ I_{OL} = 10mA	Logic "0" Output Voltage (Note 3)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V
V_{OUT} Max – V_{OUT} Common (Note 4)	Voltage Range Between Output and Common	—	—	18	—	—	18	—	—	18	V
Pulse Frequency Output Width		—	3	—	—	3	—	—	3	—	µsec

ELECTRICAL CHARACTERISTICS: (Cont.) V_{DD} = +5V, V_{SS} = – 5V, V_{GND} = 0, V_{REF} = – 5V, R_{BIAS} = 100kΩ, Full Scale = 10kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified – 40°C to +85°C for E device, 0°C to +70°C for C device.

FREQUENCY-TO-VOLTAGE		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Supply Current											
I_{DD} Quiescent (Note 5)	Current Required From Positive Supply During Operation	—	1.5	6	—	1.5	6	—	3	10	mA
I_{SS} Quiescent (Note 5)	Current Required From Negative Supply During Operation	—	– 1.5	– 6	—	– 1.5	– 6		– 3	– 10	mA
V_{DD} Supply	Operating Range of Positive Supply	4	—	7.5	4	—	7.5	4	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	– 4	—	– 7.5	– 4	—	– 7.5	– 4	—	– 7.5	V
Reference Voltage											
$V_{REF} – V_{SS}$	Range of Voltage Reference Input	– 2.5	—	—	– 2.5	—	—	– 2.5	—	—	V
Accuracy											
Nonlinearity (Note 10)	Deviation From Ideal Transfer Function as a Percentage Full-Scale Voltage	—	0.01	0.02	—	0.02	0.05	—	0.05	0.25	% Full Scale
Input Frequency Range (Note 7 and 8)	Frequency Range for Specified Nonlinearity	10	—	100k	10	—	100k	10	—	100k	Hz
Frequency Input											
Positive Excursion	Voltage Required to Turn Threshold Detector On	0.4	—	V_{DD}	0.4	—	V_{DD}	0.4	—	V_{DD}	V
Negative Excursion	Voltage Required to Turn Threshold Detector Off	– 0.4		– 2	– 0.4	—	– 2	– 0.4	—	– 2	V
Minimum Positive Pulse Width (Note 8)	Time Between Threshold Crossings	—	5	—	—	5	—	—	5	—	µsec
Minimum Negative Pulse Width (Note 8)	Time Between Threshold Crossings	—	0.5	—	—	0.5	—	—	0.5		µsec
Input Impedance		—	10	—	—	10	—	—	10	—	MΩ
Analog Outputs											
Output Voltage (Note 9)	Voltage Range of Op Amp Output for Specified Nonlinearity	—	$V_{DD} – 1$	—	—	$V_{DD} – 1$	—	—	$V_{DD} – 1$	—	V
Output Loading	Resistive Loading at Output of Op Amp	2	—	—	2	—	—	2	—	—	kΩ
Supply Current											
I_{DD} Quiescent (Note 10)	Current Required From Positive Supply During Operation	—	1.5	6	—	1.5	6	—	3	10	mA
I_{SS} Quiescent (Note 10)	Current Required From Negative Supply During Operation	—	– 1.5	– 6		– 1.5	– 6		– 3	– 10	mA
V_{DD} Supply	Operating Range of Positive Supply	4	—	7.5	4	—	7.5	4	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	– 4	—	– 7.5	– 4	—	– 7.5	– 4	—	– 7.5	V
Reference Voltage											
$V_{REF} – V_{SS}$	Range of Voltage Reference Input	– 2.5	—	—	– 2.5	—	—	– 2.5	—	—	V

NOTES:
1. Full temperature range. Guaranteed, Not Tested.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10mA.
4. I_{OUT} = 10µA.
5. Threshold Detect = 5V, Amp Out = 0V, Full Temperature Range
6. 10Hz to 100kHz.; Guaranteed, Not Tested
7. 5µsec minimum positive pulse width and 0.5 µsec minimum negative pulse width.
8. $t_R = t_F$ = 20nsec.
9. $R_L \geq$ 2kΩ.; Tested @ 10kΩ
10. Full temperature range, V_{IN} = – 0.1V.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	I_{BIAS}	This pin sets bias current in the TC9400. Connect to V_{SS} through a 100 kΩ resistor. See text.
2	Zero Adj	Low frequency adjustment input. See text.
3	I_{IN}	Input current connection for the V/F converter.
4	V_{SS}	Negative power supply voltage connection, typically – 5V.
5	V_{REF}OUT	Reference capacitor connection.
6	GND	Analog ground.
7	V_{REF}	Voltage reference input, typically – 5V.
8	Pulse Freq Out	Frequency output. This open drain output will pulse LOW each time the Freq threshold detector limit is reached. The pulse rate is proportional to input voltage.
9	Output Common	Source connection for the open drain output FETs. See text.
10	Freq/2 Out	This open drain output is a square wave at one half the frequency of the pulse output (pin 8). Output transitions of this pin occur on the rising edge of pin 8.
11	Threshold Detect	Input to the threshold detector. This pin is the frequency input during F/V operation.
12	Amplifier Out	Output of the integrator amplifier.
13	NC	No internal connection
14	V_{DD}	Positive power supply connection, typically +5V.

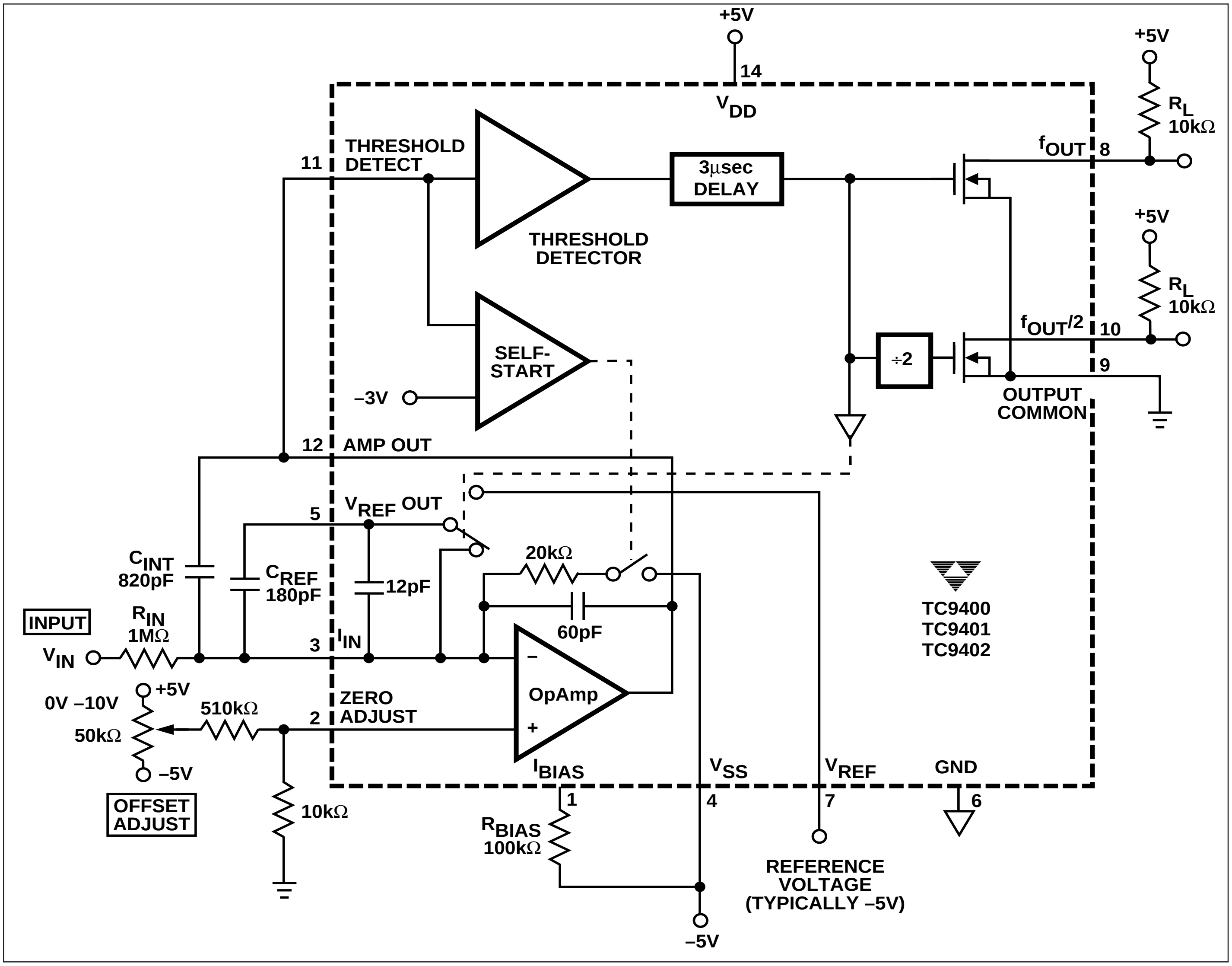
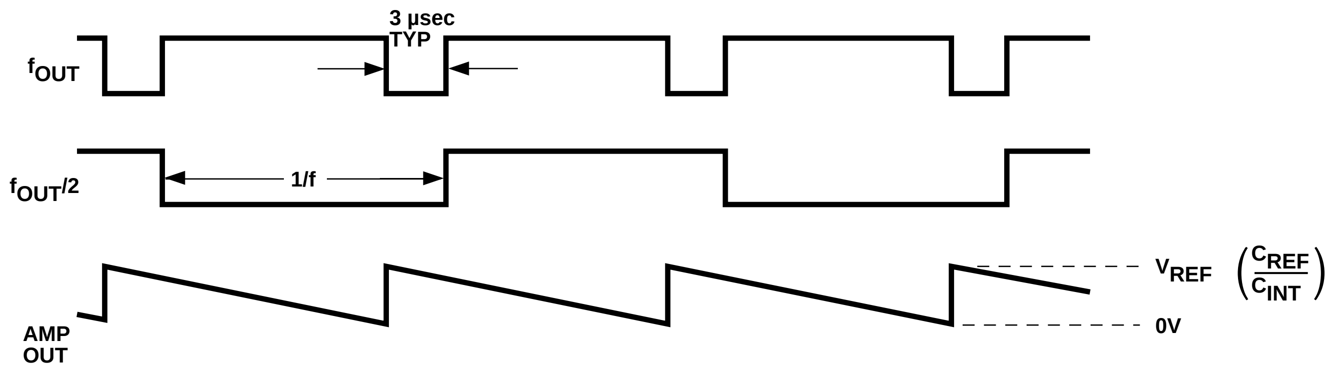


Figure 1. 10 Hz to 10 kHz V/F Converter

VOLTAGE-TO-FREQUENCY (V/F) CIRCUIT DESCRIPTION

The TC9400 V/F converter operates on the principal of charge balancing. The operation of the TC9400 is easily understood by referring to Figure 1. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge on the integrating capacitor and shows up as a linearly decreasing voltage at the output of the op amp. The lower limit of the output swing is set by the threshold detector, which causes the reference voltage to be applied to the reference capacitor for a time period long enough to charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$), causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out. This dissipates the charge stored on the reference capacitor, so that when the output again crosses zero the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, which causes the output frequency to also increase. Since each charge increment is fixed, the increase in frequency with voltage is linear. In addition, the accuracy of the output pulse width does not directly affect the linearity of the V/F. The pulse must simply be long enough for full charge transfer to take place.



NOTES: 1. To adjust f_{MIN}, set V_{IN} = 10mV and adjust the 50kΩ offset for 10Hz output.
2. To adjust f_{MAX}, set V_{IN} = 10V and adjust R_{IN} or V_{REF} for 10 kHz output.
3. To increase f_{OUT} MAX to 100kHz, change C_{REF} to 2pF and C_{INT} to 75pF.
4. For high-performance applications, use high-stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass capacitors). Also, separate output ground (pin 9) from input ground (pin 6).

Figure 2 . Output Waveforms

The TC9400 contains a "self-start" circuit to ensure the V/F converter always operates properly when power is first applied. In the event that, during power-on, the Op amp output is below the threshold and C_{REF} is already charged, a positive voltage step will not occur. The op-amp output will continue to decrease until it crosses the –3.0V threshold of the "self-start" comparator. When this happens, an internal resistor is connected to the op-amp input, which forces the output to go positive until the TC9400 is in its normal operating mode.

The TC9400 utilizes low power CMOS processing for low input bias and offset currents with very low power dissipation. The open-drain N-channel output FETs provide high voltage and high current sink capability.

VOLTAGE-TO-TIME MEASUREMENTS

The TC9400 output can be measured in the time domain as well as the frequency domain. Some microcomputers, for example, have extensive timing capability but limited counter capability. Also, the response time of a time domain measurement is only the period between two output pulses, while the frequency measurement must accumulate pulses during the entire counter timebase period.

Time measurements can be made from either the TC9400's Pulse Freq Out output or from the Freq/2 output. The Freq/2 output changes state on the rising edge of Pulse Freq Out, so Freq/2 is a symmetrical square wave at one half the pulse output frequency. Timing measurements can therefore be made between successive Pulse Freq Out pulses, or while Freq/2 is high (or low).

PIN FUNCTIONS

Threshold Detector Input

In the V/F mode, this input is connected to the amplifier output (pin 12) and triggers a 3 μsec pulse when the input voltage passes through its threshold. In the F/V mode, the input frequency is applied to this input.

The nominal threshold of the detector is halfway between the power supplies, or $(V_{DD} + V_{SS})/2 \pm 400$mV. The TC9400's charge balancing V/F technique is not dependent on a precision comparator threshold, because the threshold only sets the lower limit of the op-amp output. The op-amp's peak-to-peak output swing, which determines the frequency, is only influenced by external capacitors and by V_{REF}.

Pulse Freq Out

This output is an open-drain N-channel FET which provides a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Freq/2 Out

This output is an open-drain N-channel FET which provides a square wave one-half the frequency of the pulse frequency output. The Freq/2 output will change state on the rising edge of Pulse Freq Out. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common

The sources of both the Freq/2 out and the Pulse Freq Out are connected to this pin. An output level swing from the drain voltage to ground or to the V_{SS} supply may be obtained by connecting this pin to the appropriate point.

R_{BIAS}

An external resistor, connected to V_{SS}, sets the bias point for the TC9400. Specifications for the TC9400 are based on R_{BIAS} = 100kΩ ±10%, unless otherwise noted.

Increasing the maximum frequency of the TC9400 beyond 100kHz is limited by the pulse width of the Pulse Output (typically 3µsec). Reducing R_{BIAS} will decrease the pulse width and increase the maximum operating frequency, but linearity errors will also increase. R_{BIAS} can be reduced to 20kΩ, which will typically produce a maximum full scale frequency of 500kHz.

Amplifier Out

The output stage of the operational amplifier. During V/F operation, a negative-going ramp signal is available at this pin. In the F/V mode, a voltage proportional to the frequency input is generated.

Zero Adjust

This pin is the noninverting input of the operational amplifier. The low-frequency set point is determined by adjusting the voltage at this pin.

I_{IN}

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10µA is specified, but an overrange current up to 50µA can be used without detrimental effect to the circuit operation. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

V_{REF}

A reference voltage from either a precision source or the V_{SS} supply is applied to this pin. Accuracy of the TC9400 is dependent on the voltage regulation and temperature characteristics of the reference circuitry.

Since the TC9400 is a charge balancing V/F converter, the reference current will be equal to the input current. For this reason, the DC impedance of the reference voltage source must be kept low enough to prevent linearity errors. For linearity of 0.01%, a reference impedance of 200Ω or less is recommended. A 0.1µF bypass capacitor should be connected from V_{REF} to ground.

V_{REF} Out

The charging current for C_{REF} is supplied through this pin. When the op amp output reaches the threshold level, this pin is internally connected to the reference voltage and a charge, equal to $V_{REF} \times C_{REF}$, is removed from the integrator capacitor. After about 3 µsec, this pin is internally connected to the summing junction of the op amp to discharge C_{REF}. Break-before-make switching ensures that the reference voltage is not directly applied to the summing junction.

V/F CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output frequency (f_{OUT}) is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\,(C_{REF})}$$

External Component Selection

R_{IN}

The value of this component is chosen to give a full-scale input current of approximately 10µA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\mu A}.$$

Example: $$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega.$$

Note that the value is an approximation and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full-scale frequency at V_{IN} full scale (see "Adjustment Procedure"). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

C_{INT}

The exact value is not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10\ C_{REF}.$$

Improved stability and linearity are obtained when $C_{INT} \leq 4C_{REF}$. Low-leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 13.

C_{REF}

The exact value is not critical and may be used to trim the full-scale frequency (see "Input/Output Relationships"). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended. For high-accuracy requirements, 0.05% line and load regulation and 0.1µF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure

Figure 1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure for a 10kHz full-scale frequency is as follows:

(1) Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10Hz output frequency.

(2) Set V_{IN} to 10V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10kHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

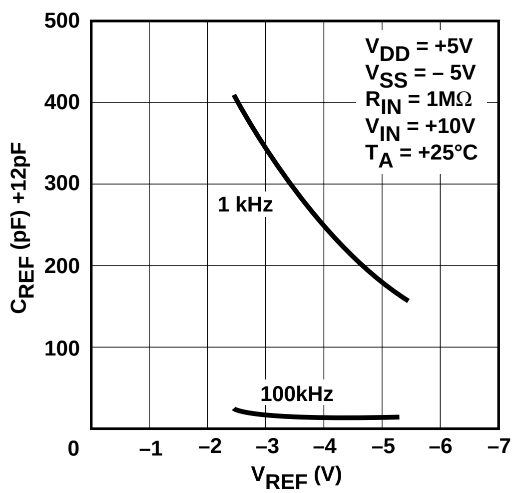


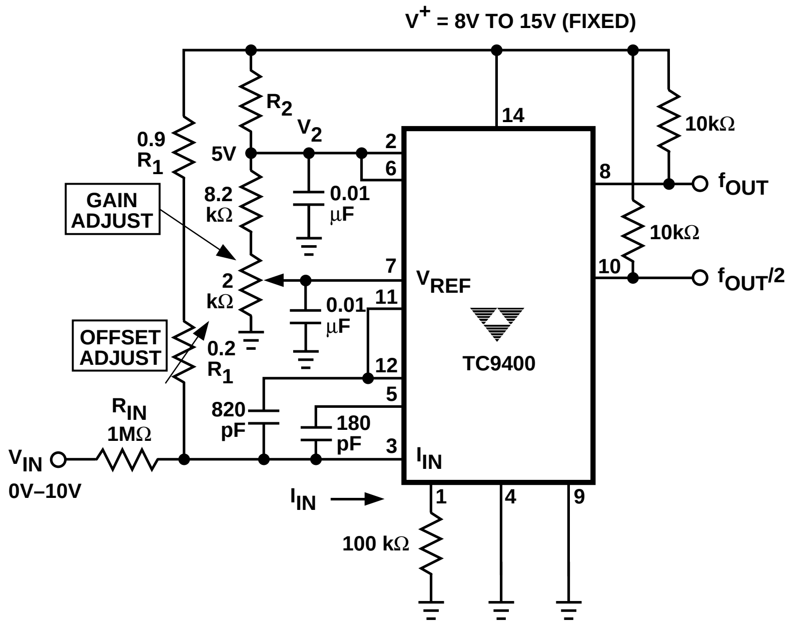
Figure 3. Recommended C_{REF} vs V_{REF}

Improved Single Supply V/F Converter Operation

A TC9400 which operates from a single 12 to 15V variable power source is shown in Figure 5. This circuit uses two Zener diodes to set stable biasing levels for the TC9400. The Zener diodes also provide the reference voltage, so the output impedance and temperature coefficient of the Zeners will directly affect power supply rejection and temperature performance.

Full scale adjustment is accomplished by trimming the input current. Trimming the reference voltage is not recommended for high accuracy applications unless an op amp is used as a buffer, because the TC9400 requires a low impedance reference (see the V_{REF} pin description section for more information).

The circuit of Figure 5 will directly interface with CMOS logic operating at 12V to 15V. TTL or 5V CMOS logic can be accommodated by connecting the output pullup resistors to the +5V supply. An optoisolator can also be used if an isolated output is required.

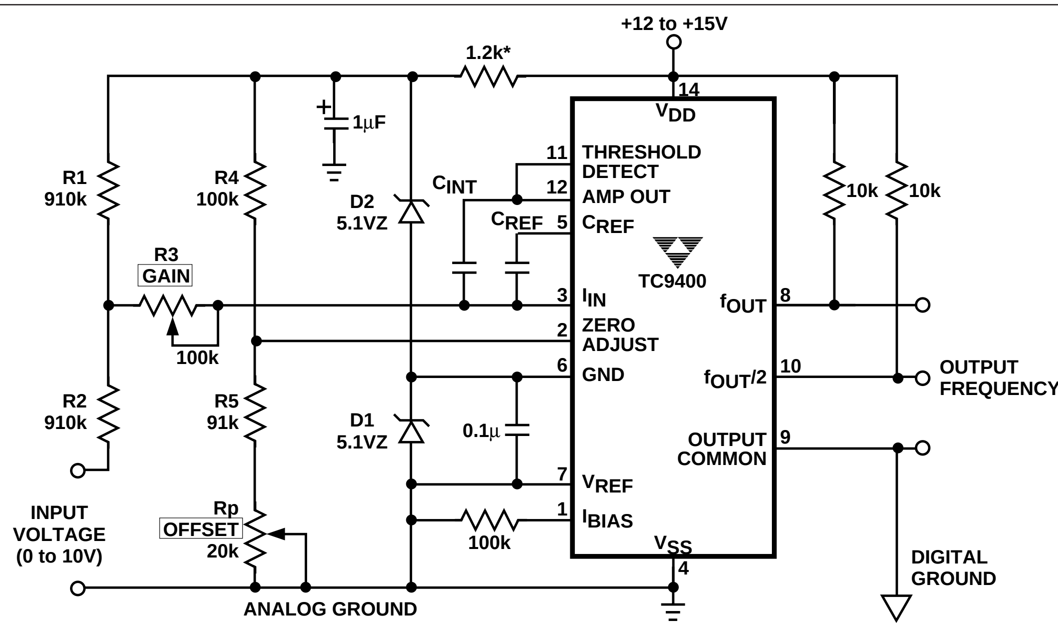


V^+	R_1	R_2
10V	1 MΩ	10kΩ
12V	1.4 MΩ	14kΩ
15V	2 MΩ	20kΩ

$$f_{OUT} = I_{IN} \times \frac{1}{(V_2 - V_7)\,(C_{REF})}$$

$$I_{IN} = \frac{(V_{IN} - V_2)}{R_{IN}} + \frac{(V^+ - V_2)}{(0.9\,R_1 + 0.2\,R_1)}$$

Figure 4 . Fixed Voltage — Single Supply Operation



COMPONENT SELECTION

F/S FREQ.	CREF	CINT
1 kHz	2200pF	4700pF
10 kHz	180pF	470pF
100 kHz	27pF	75pF

Figure 5. Voltage to Frequency

FREQUENCY-TO-VOLTAGE (F/V) CIRCUIT DESCRIPTION

When used as an F/V converter, the TC9400 generates an output voltage linearly proportional to the input frequency waveform.

Each zero crossing at the threshold detector's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor, generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

F/V CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output voltage is related to the input frequency (f_{IN}) by the transfer equation:

$$V_{OUT} = [V_{REF}\ C_{REF}\ R_{INT}]\ f_{IN}.$$

The response time to a change in f_{IN} is equal to (R_{INT} C_{INT}). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the input frequency.

C_{INT} can be increased to lower the ripple. Values of 1µF to 100µF are perfectly acceptable for low frequencies.

When the TC9400 is used in the single-supply mode, V_{REF} is defined as the voltage difference between pin 7 and pin 2.

Input Voltage Levels

The input frequency is applied to the Threshold Detector input (Pin 11). As discussed in the V/F circuit section of this data sheet, the threshold of pin 11 is approximately (V_{DD} + V_{SS}) /2 ±400mV. Pin 11's input voltage range extends from V_{DD} to about 2.5 V below the threshold. If the voltage on pin 11 goes more than 2.5 volts below the threshold, the V/F mode startup comparator will turn on and corrupt the output voltage. The Threshold Detector input has about 200 mV of hysteresis.

In ±5 V applications, the input voltage levels for the TC9400 are ±400mV, minimum. If the frequency source being measured is unipolar, such as TTL or CMOS operating from a +5V source, then an AC coupled level shifter should be used. One such circuit is shown in Figure 6a.

The level shifter circuit in Figure 6b can be used in single supply F/V applications. The resistor divider ensures that the input threshold will track the supply voltages. The diode clamp prevents the input from going far enough in the negative direction to turn on the startup comparator. The diode's forward voltage decreases by 2.1 mV/°C, so for high ambient temperature operation two diodes in series are recommended.

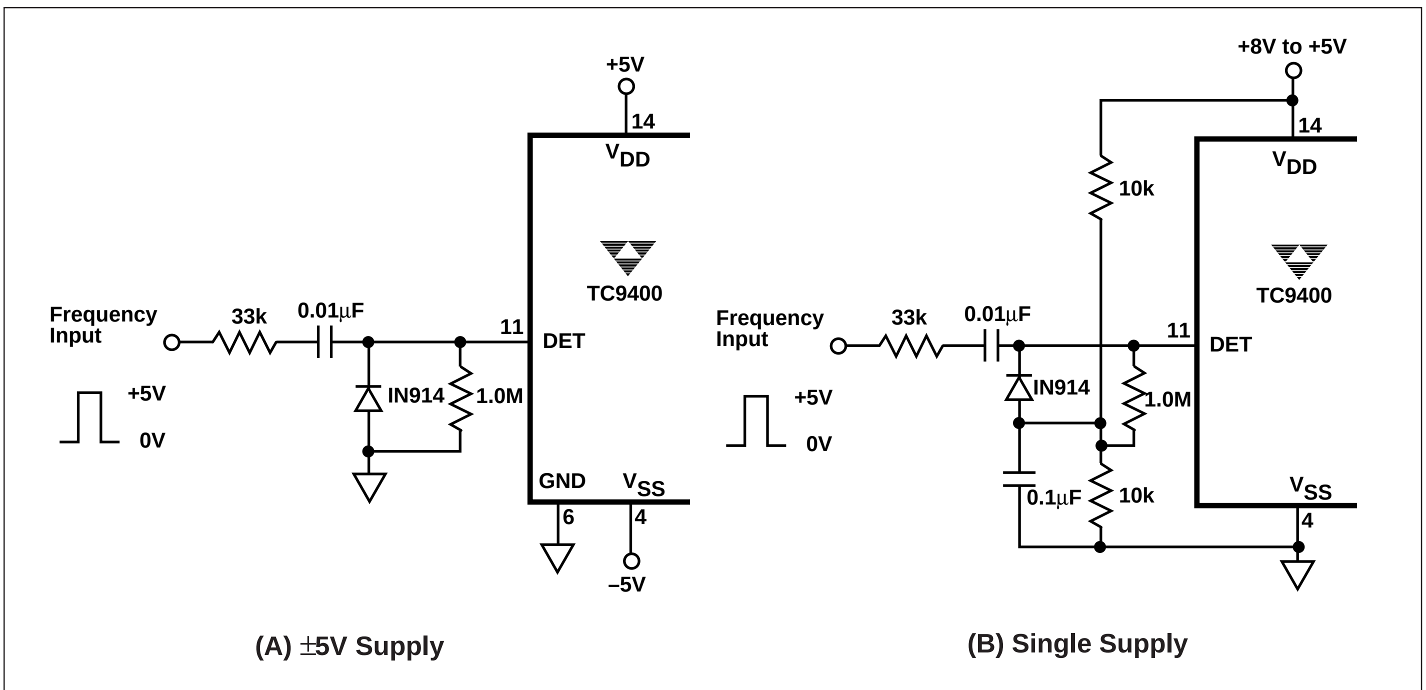


Figure 6. Frequency Input Level Shifter

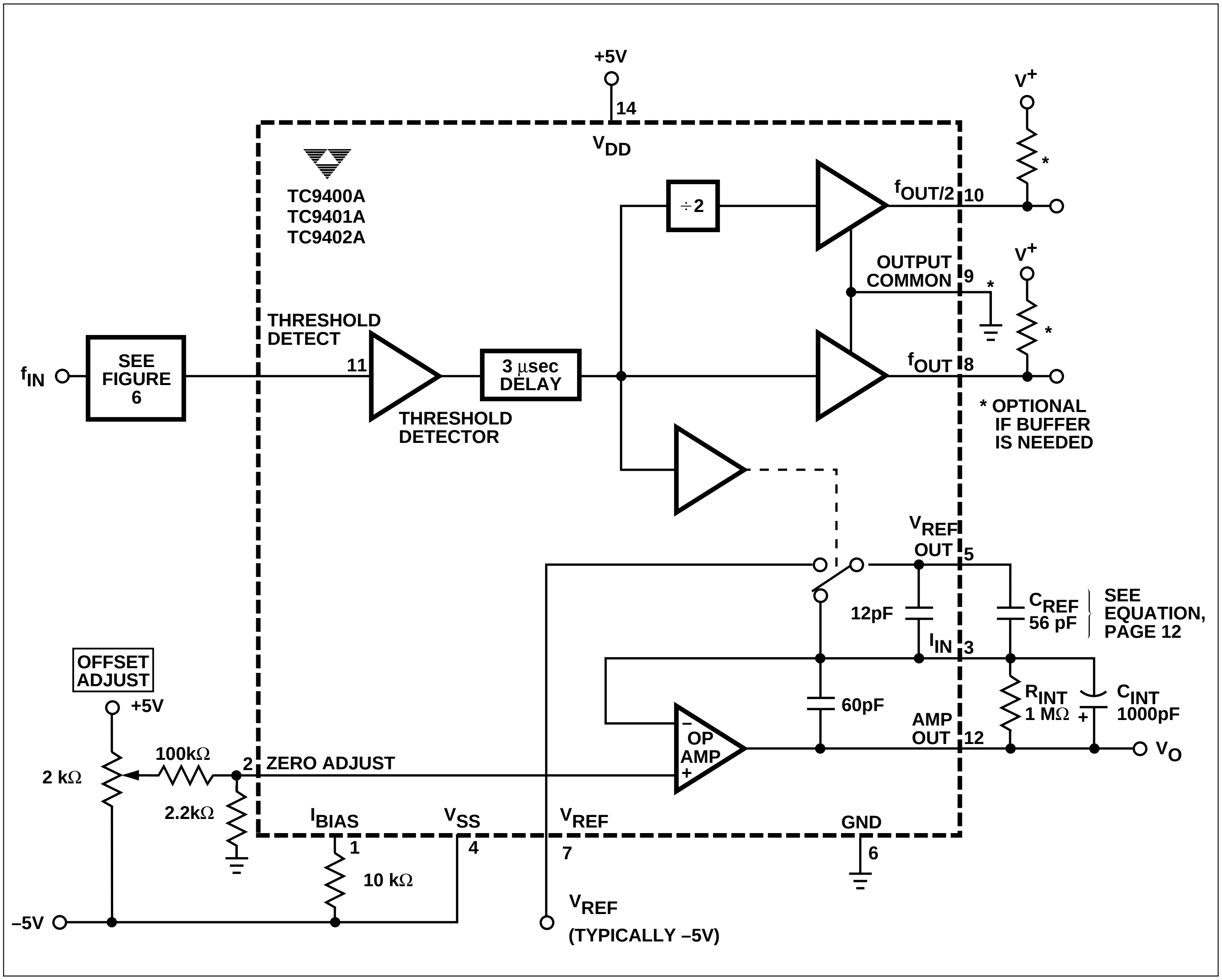


Figure 7. DC — 10 kHz F/V Converter

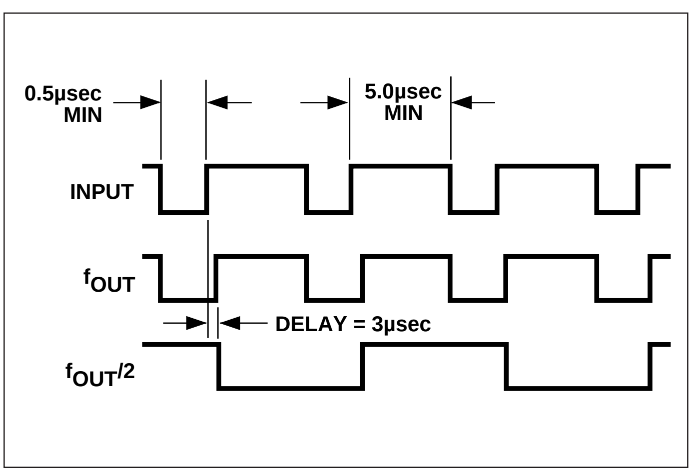
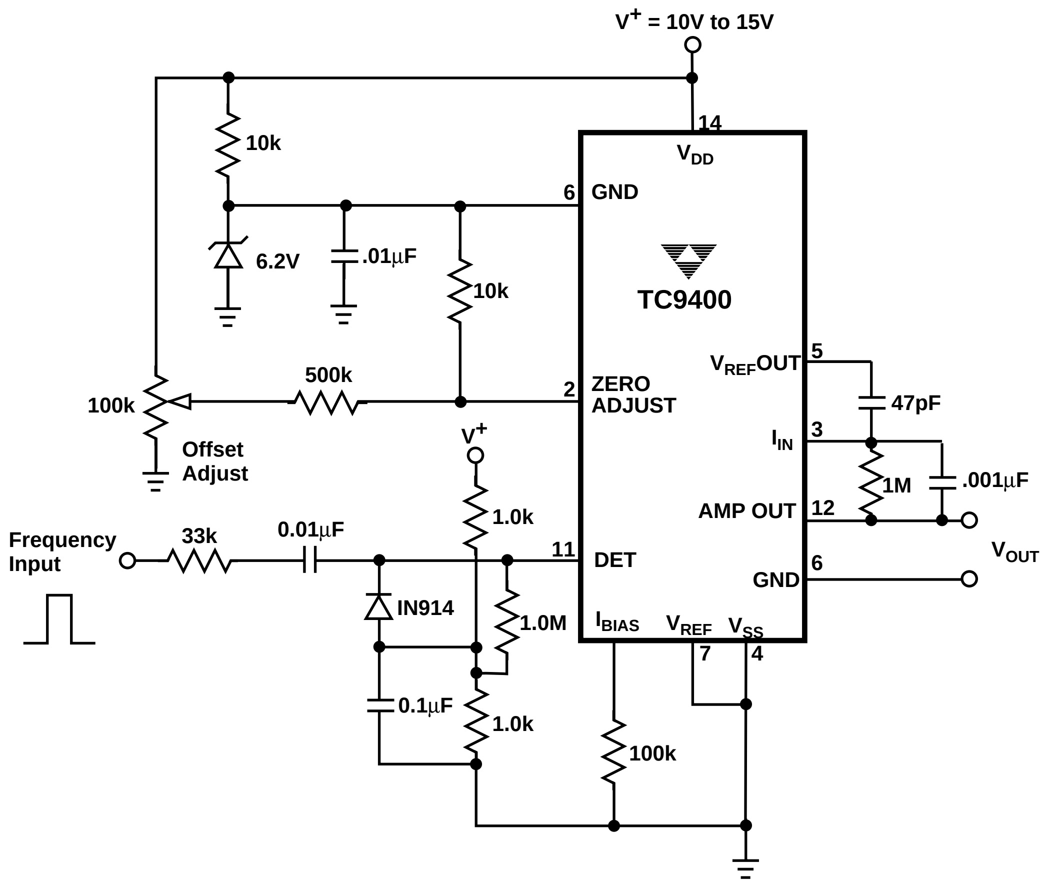


Figure 8 . F/V Digital Outputs

Input Buffer

f_{OUT} and $f_{OUT}/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. Then, f_{OUT} will follow the input frequency waveform, except that f_{OUT} will go high 3µsec after f_{IN} goes high; $f_{OUT}/2$ will be squarewave with a frequency of one-half f_{OUT}.

If these outputs are not used, pins 8, 9 and 10 should be connected to ground.



Note: The output is referenced to pin 6, which is at 6.2V (Vz). For frequency meter applications, a 1 mA meter with a series-scaling resistor can be placed across pins 6 and 12.

Figure 9. F/V Single Supply F/V Converter

Output Filtering

The output of the TC9400 has a sawtooth ripple superimposed on a DC level. The ripple will be rejected if the TC9400 output is converted to a digital value by an integrating analog to digital converter, such as the TC7107 or TC7109. The ripple can also be reduced by increasing the value of the integrating capacitor, although this will reduce the response time of the F/V converter.

The sawtooth ripple on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit is a capacitance multiplier, where the output coupling capacitor is multiplied by the AC gain of the op amp. A moderately fast op amp, such as the TL071, should be used.

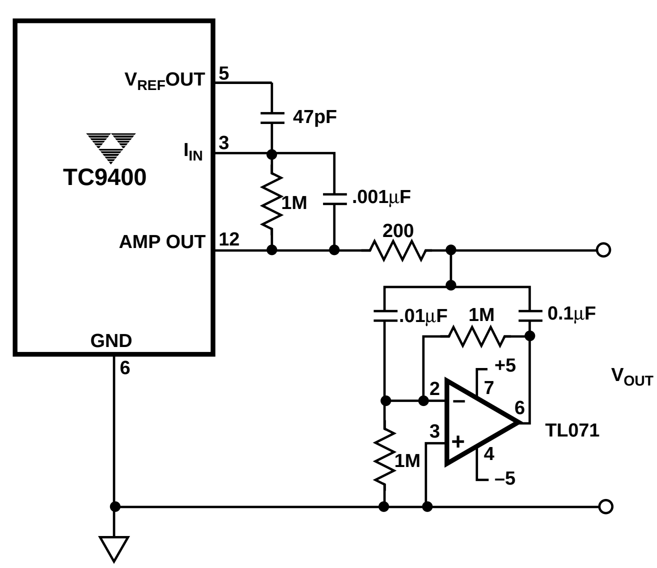


Figure 10. Ripple Filter

F/V POWER-ON RESET

In F/V mode, the TC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition remains until the first pulse is applied to f_{IN}. In most frequency-measurement applications this is not a problem, because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from pin 11 to V_{DD} will usually be sufficient to pulse the TC9400 and provide a power-on reset (see Figure 11A). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 11B, may be required.

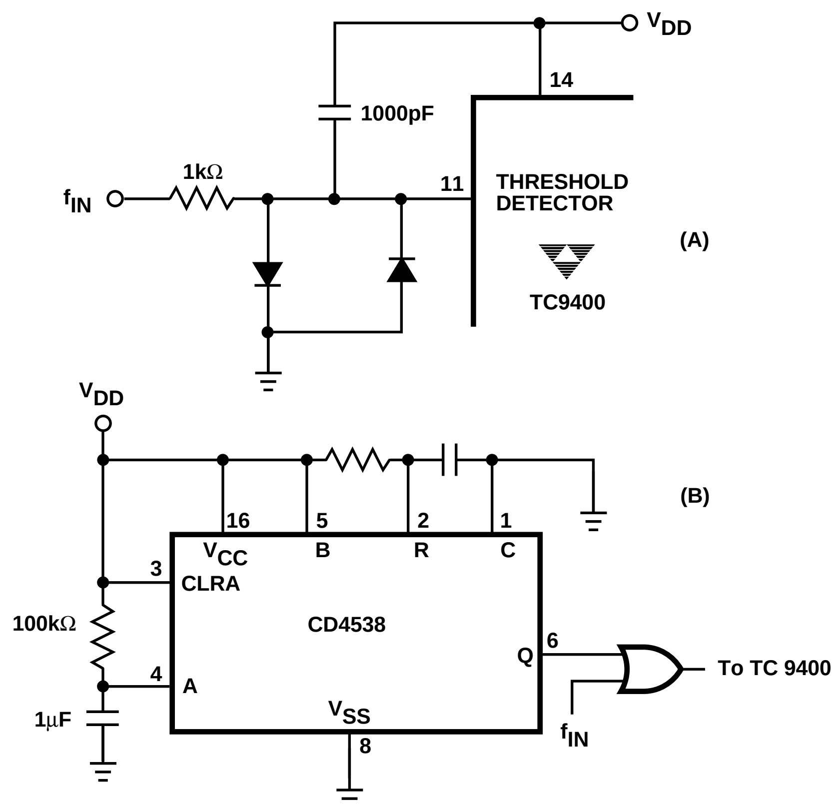
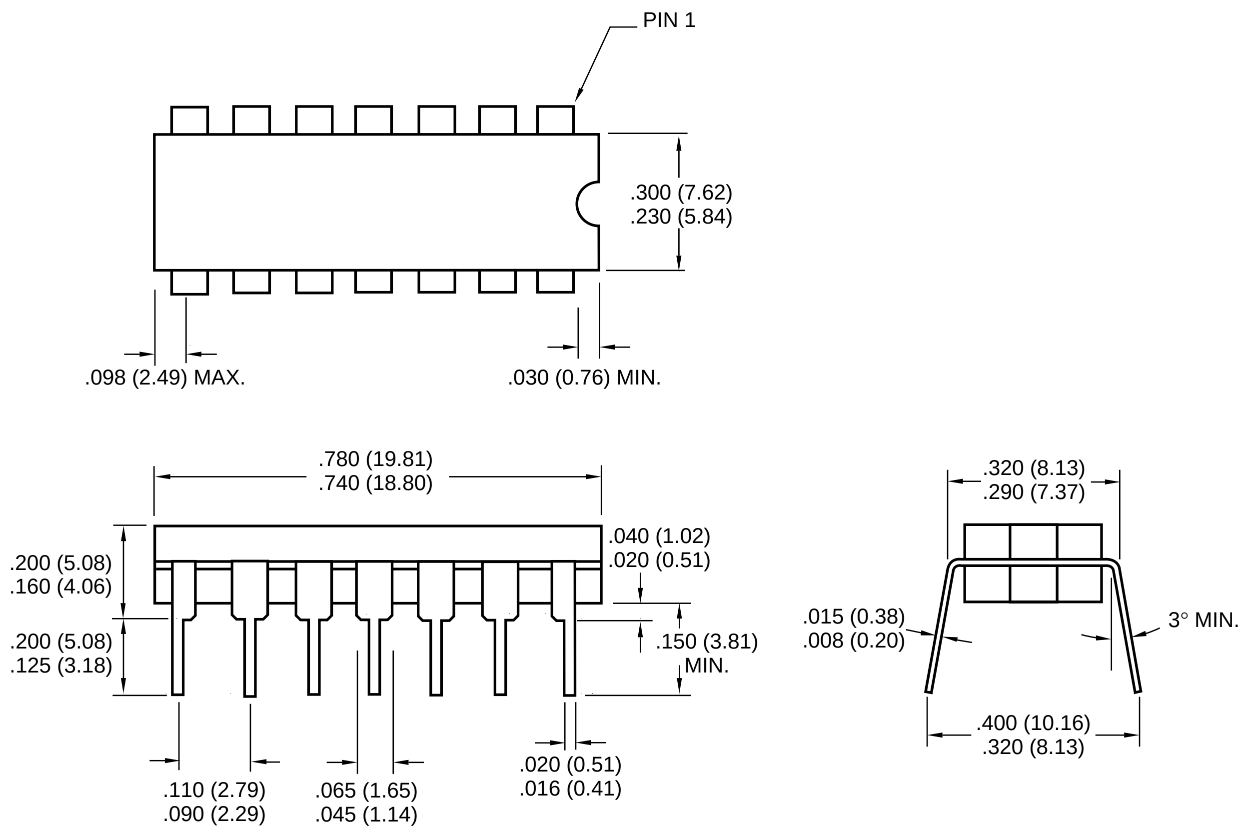


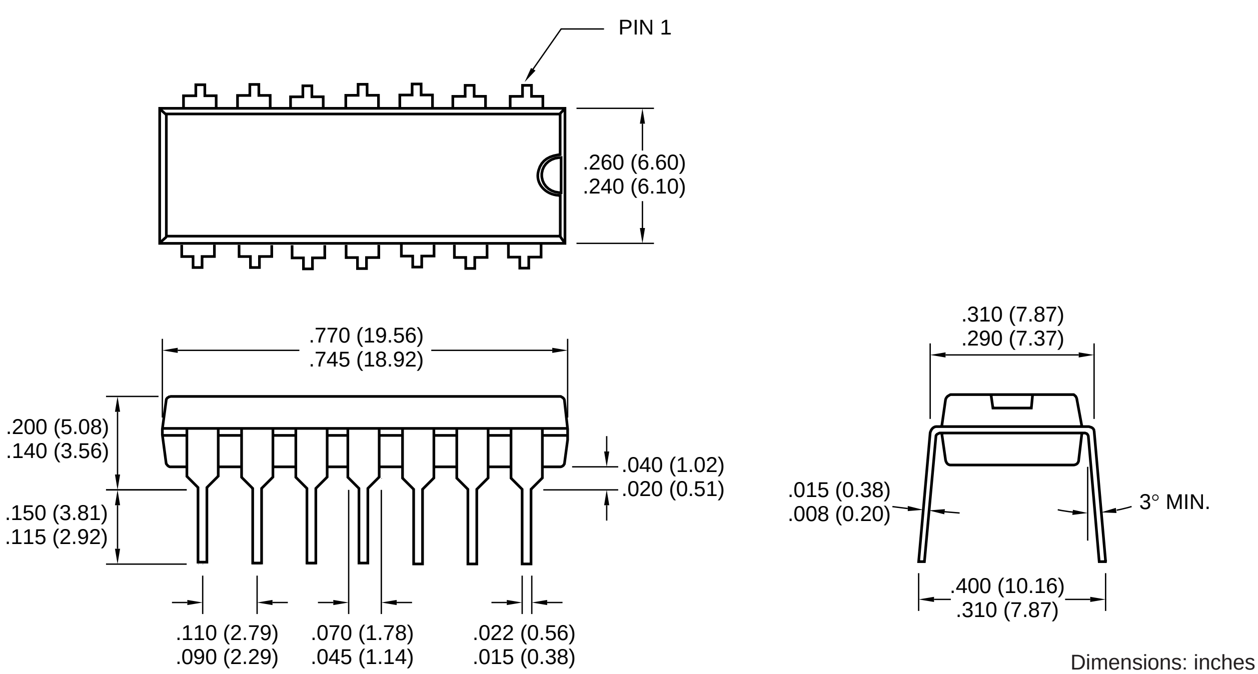
Figure 11. Power-On Operation/Reset

PACKAGE DIMENSIONS

14-Pin CerDIP



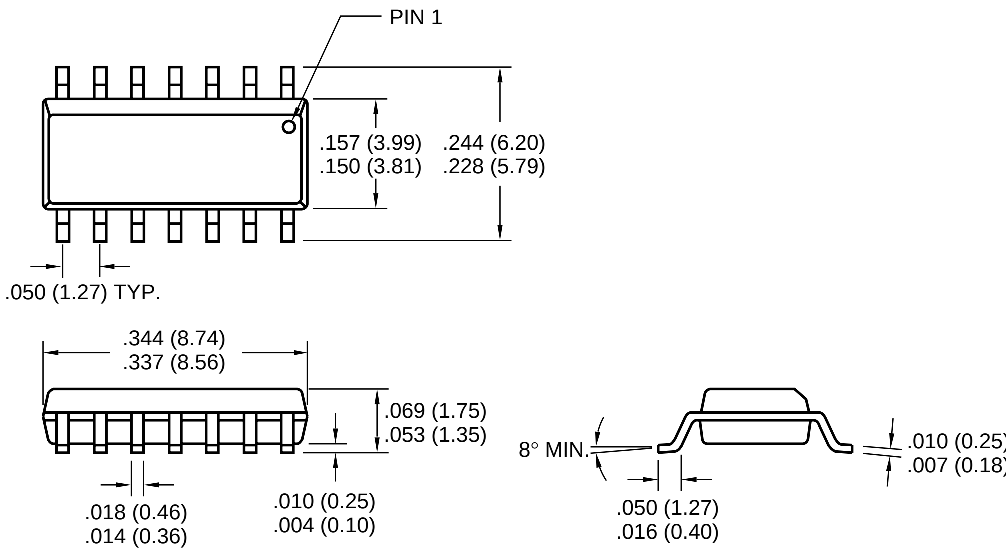
14-Pin Plastic DIP



Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

14-Pin SOIC (Narrow)



Dimensions: inches (mm)

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